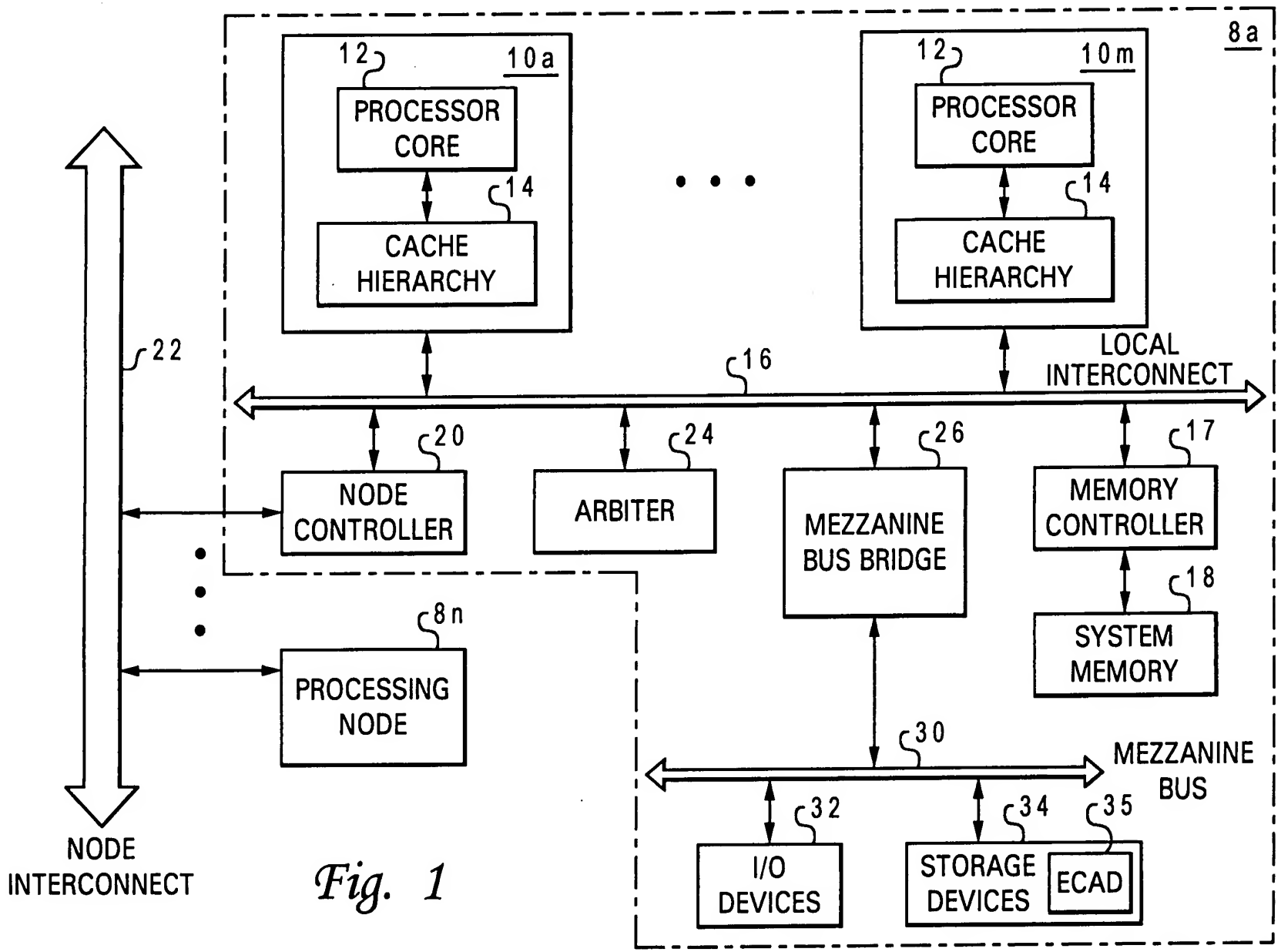
8a
12
10a
PROCESSOR CORE
14
CACHE HIERARCHY
12
10m
PROCESSOR CORE
14
CACHE HIERARCHY
22
16
LOCAL INTERCONNECT
20
24
26
17
NODE CONTROLLER
ARBITER
MEZZANINE BUS BRIDGE
MEMORY CONTROLLER
18
SYSTEM MEMORY
8n
PROCESSING NODE
30
MEZZANINE BUS
32
34
35
I/O DEVICES
STORAGE DEVICES
ECAD
NODE INTERCONNECT
12a

Fig. 1

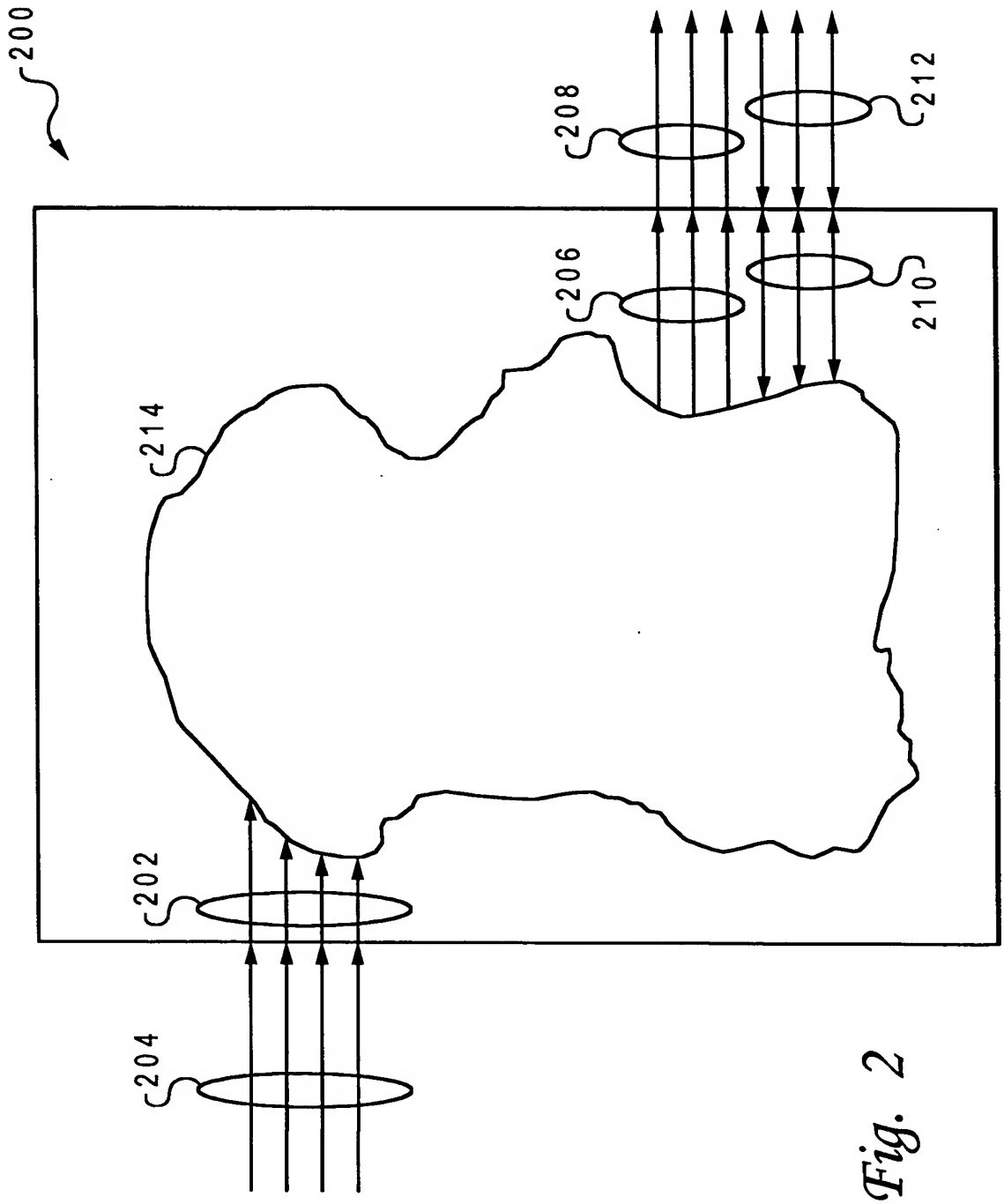

Fig. 2

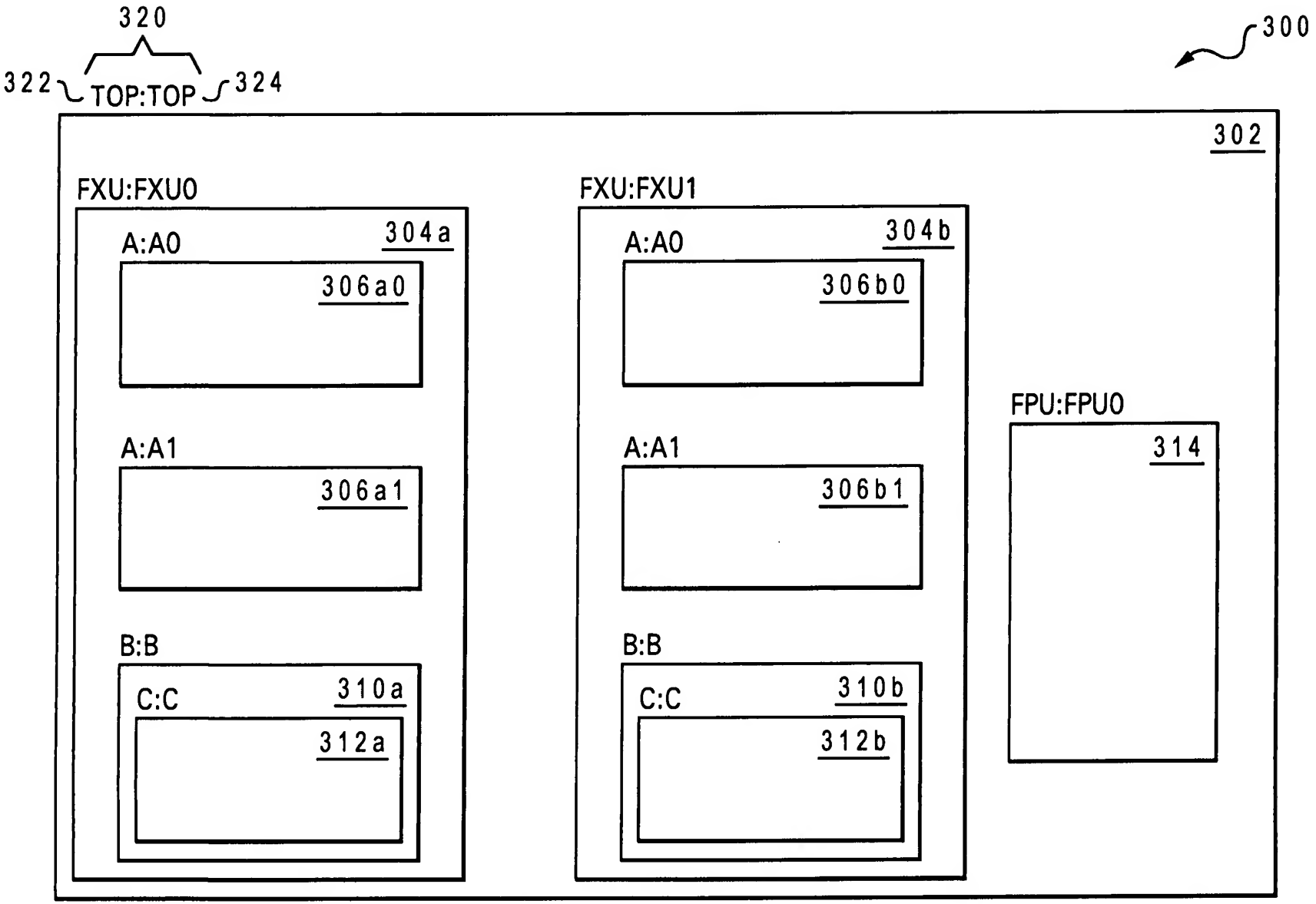
320
322
TOP:TOP
324
300
302
FXU:FXU0
A:A0
304a
306a0
A:A1
306a1
B:B
C:C
310a
312a
FXU:FXU1
A:A0
304b
306b0
A:A1
306b1
B:B
C:C
310b
312b
FPU:FPU0
314

Fig. 3

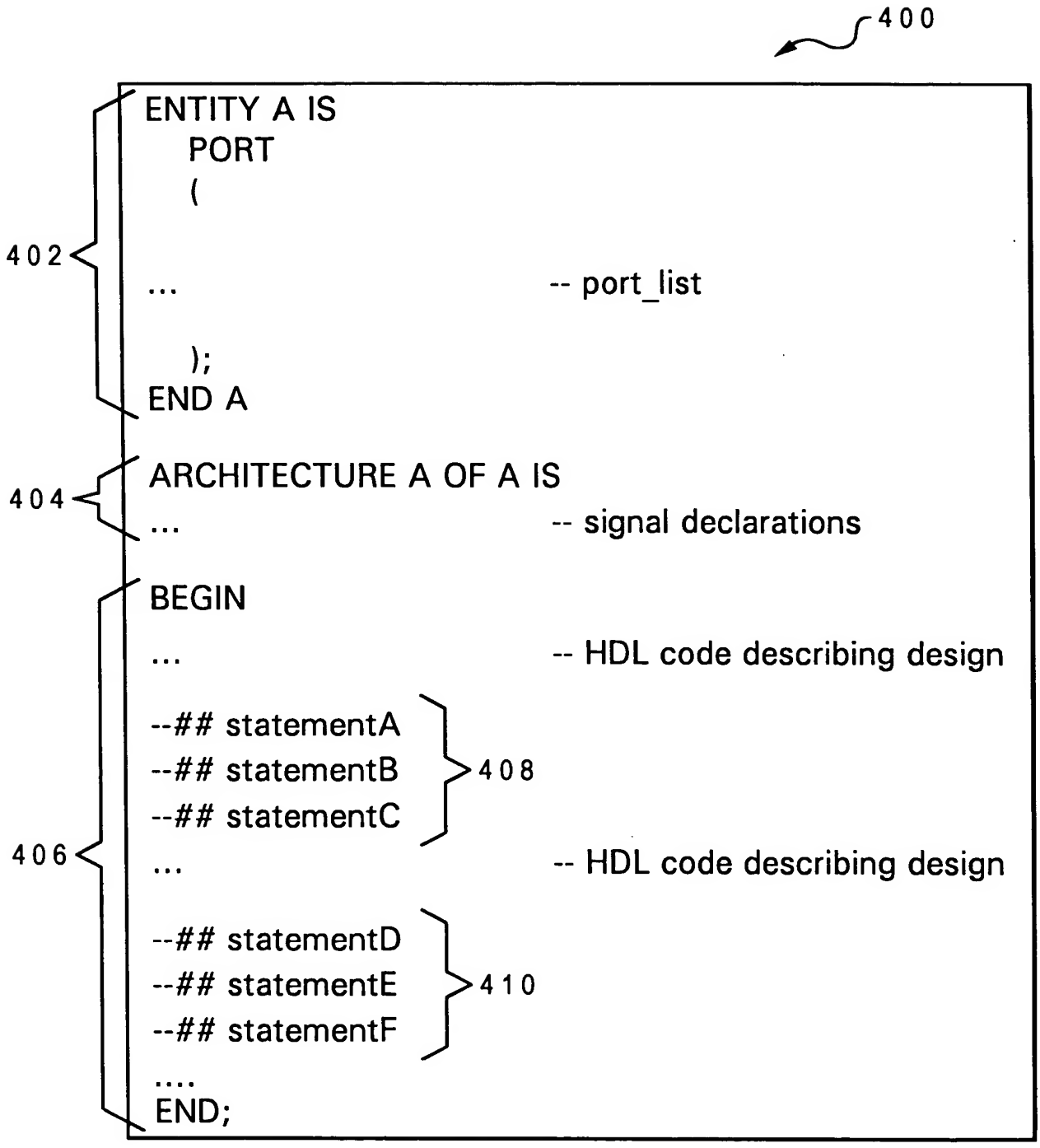
400
ENTITY A IS
PORT
(
...
-- port_list
);
END A
ARCHITECTURE A OF A IS
...
-- signal declarations
BEGIN
...
-- HDL code describing design
--## statementA
--## statementB
--## statementC
...
-- HDL code describing design
--## statementD
--## statementE
--## statementF
....
END;
402
404
406
408
410

Fig. 4A

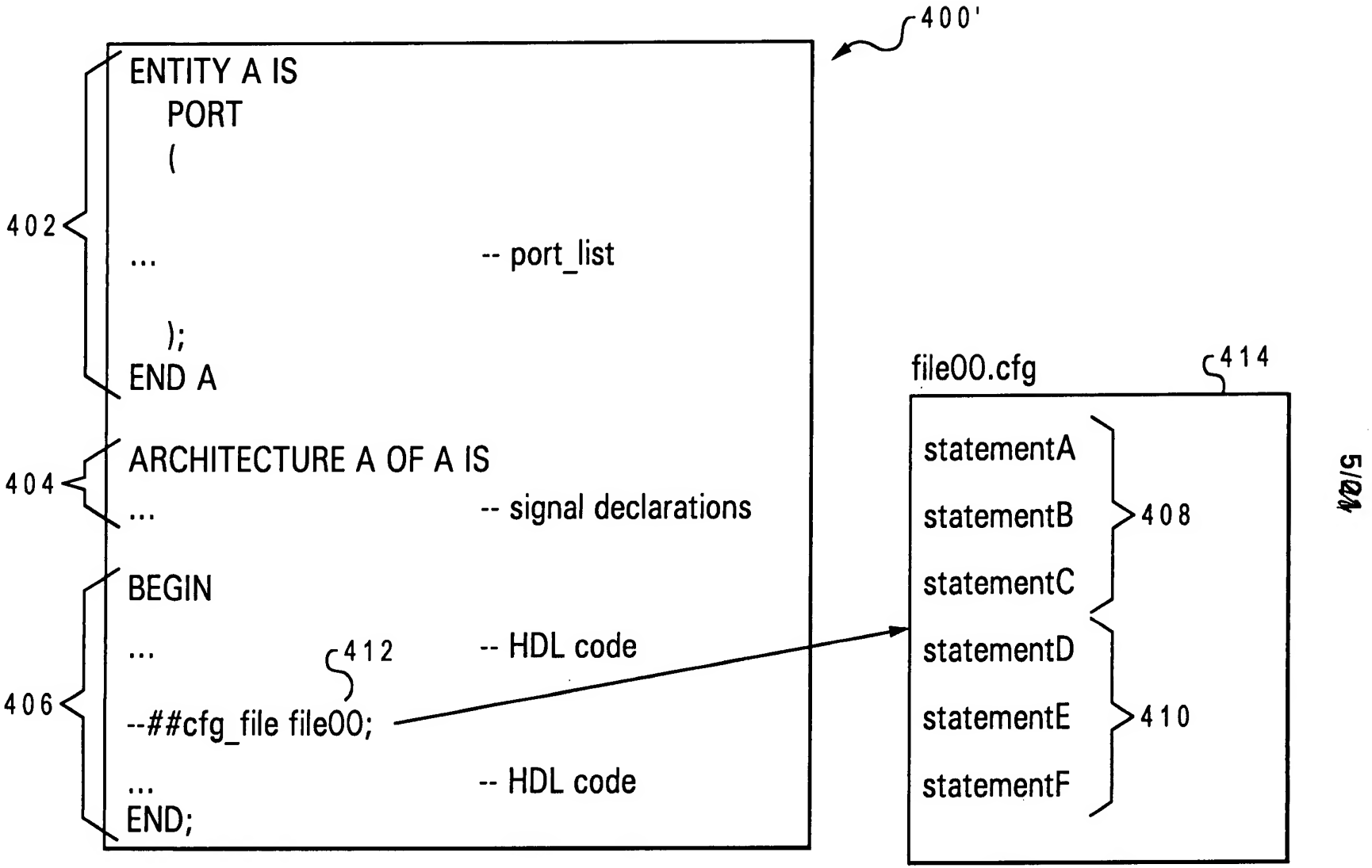
400'
ENTITY A IS
PORT
(
...
-- port_list
);
END A
ARCHITECTURE A OF A IS
...
-- signal declarations
BEGIN
...
-- HDL code
412
--##cfg_file file00;
...
-- HDL code
END;
402
404
406
file00.cfg
414
statementA
statementB
statementC
statementD
statementE
statementF
408
410
5/0A

Fig. 4B

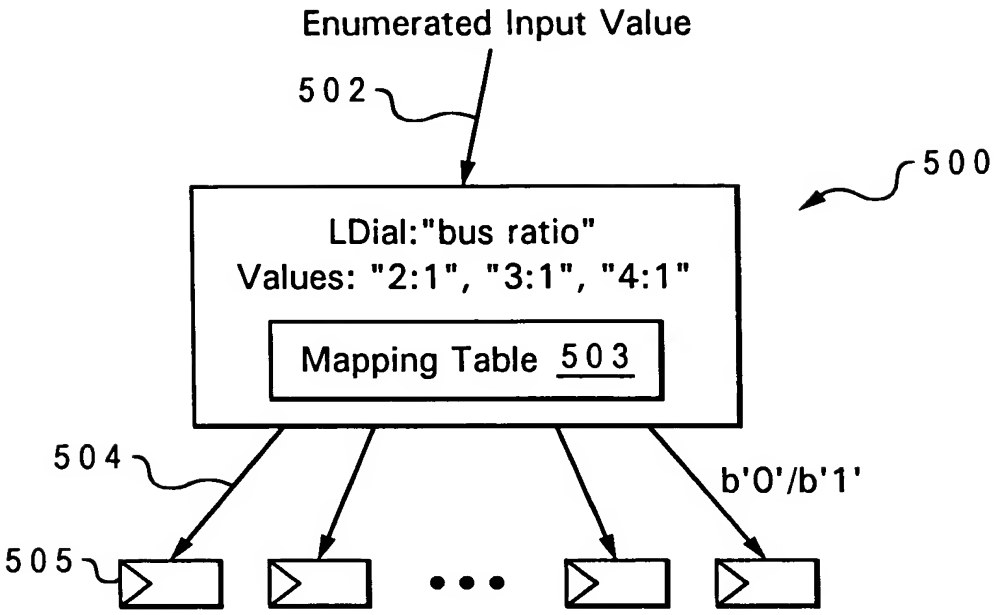
Enumerated Input Value
502
500
LDial:"bus ratio"
Values: "2:1", "3:1", "4:1"
Mapping Table 503
504
b'0'/b'1'
505

Fig. 5A

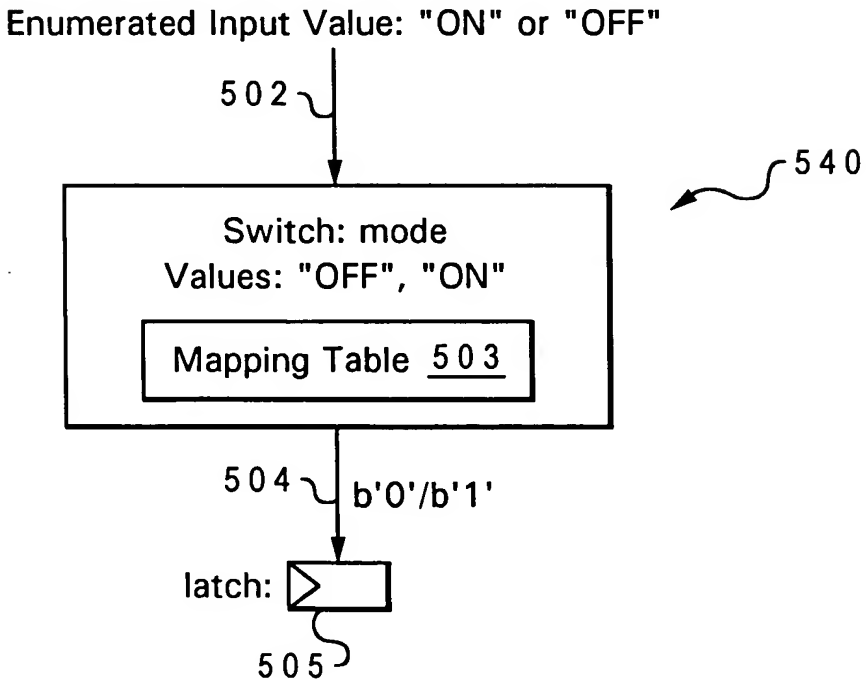
Enumerated Input Value: "ON" or "OFF"
502
540
Switch: mode
Values: "OFF", "ON"
Mapping Table 503
504
b'0'/b'1'
latch:
505

Fig. 5D

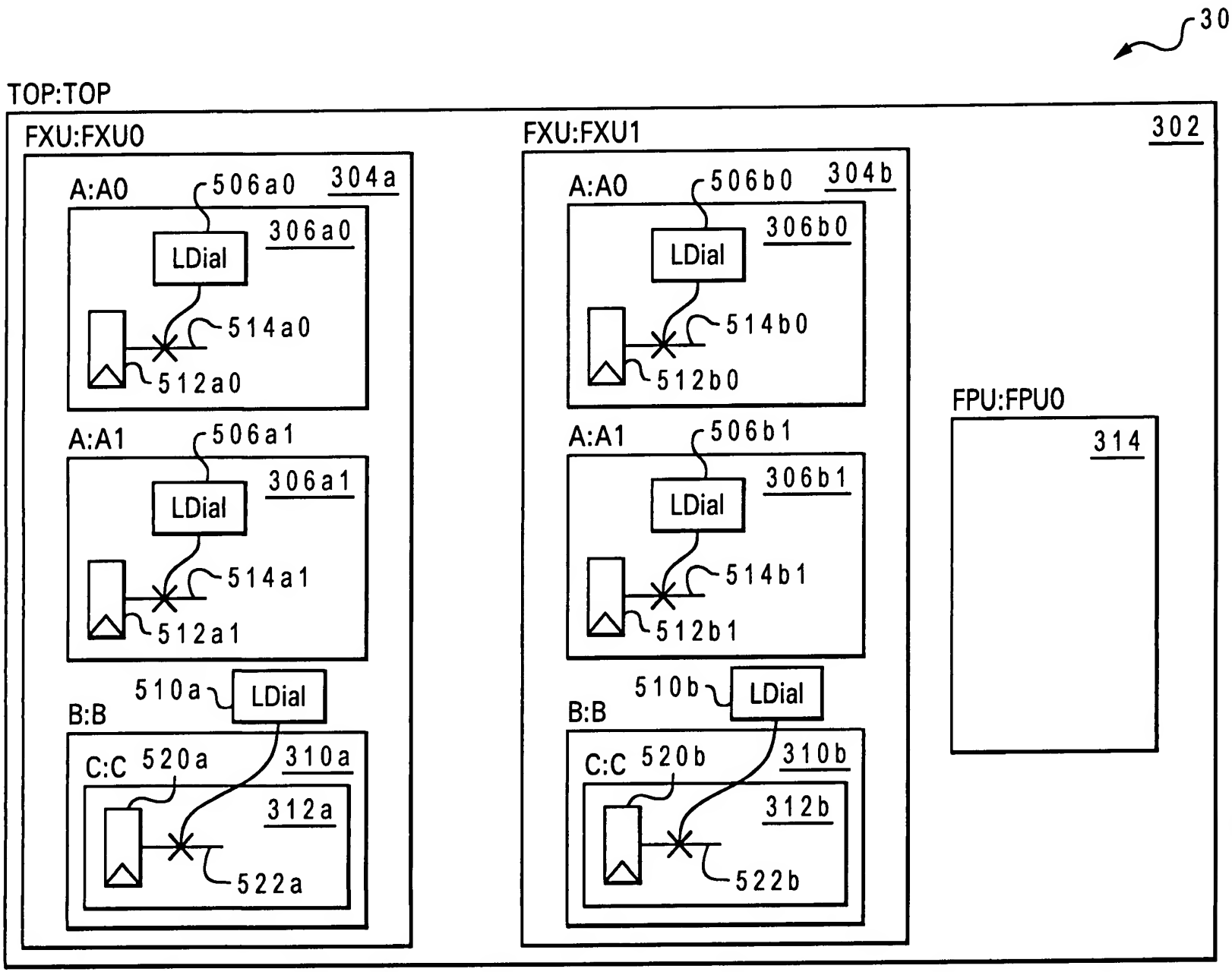
300'
TOP:TOP
FXU:FXU0
A:A0
506a0
304a
306a0
LDial
514a0
512a0
A:A1
506a1
306a1
LDial
514a1
512a1
510a
LDial
B:B
C:C
520a
310a
312a
522a
FXU:FXU1
302
A:A0
506b0
304b
306b0
LDial
514b0
512b0
A:A1
506b1
306b1
LDial
514b1
512b1
510b
LDial
B:B
C:C
520b
310b
312b
522b
FPU:FPU0
314

Fig. 5B

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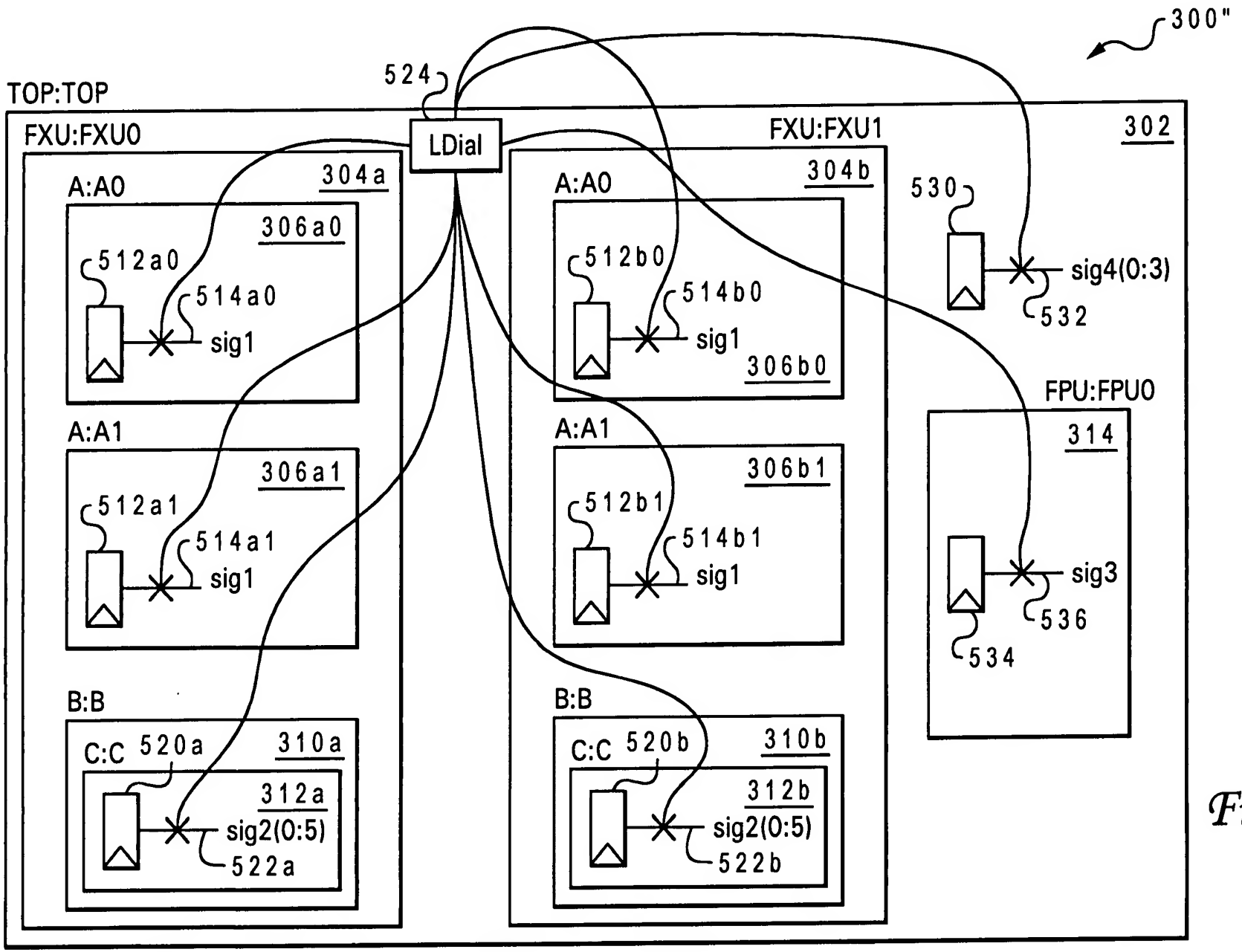
300"
524
TOP:TOP
FXU:FXU0
LDial
FXU:FXU1
302
A:A0
304a
306a0
512a0
514a0
sig1
A:A1
306a1
512a1
514a1
sig1
B:B
C:C
520a
310a
312a
sig2(0:5)
522a
A:A0
304b
512b0
514b0
sig1
306b0
A:A1
306b1
512b1
514b1
sig1
B:B
C:C
520b
310b
312b
sig2(0:5)
522b
530
sig4(0:3)
532
FPU:FPU0
314
sig3
536
534

Fig. 5C

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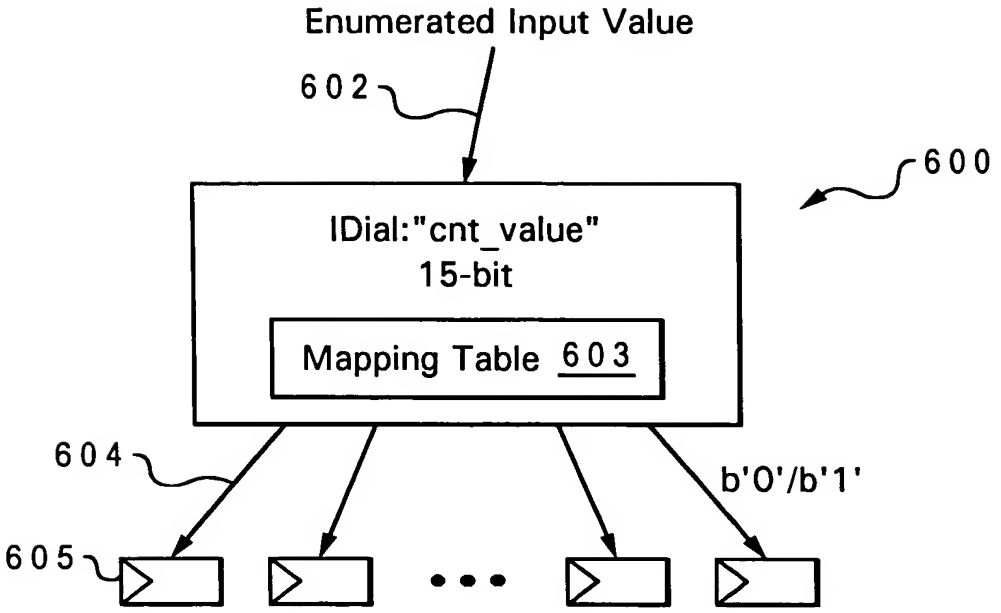

Enumerated Input Value
602
600
IDial:"cnt_value"
15-bit
Mapping Table 603
604
b'0'/b'1'
605

Fig. 6A

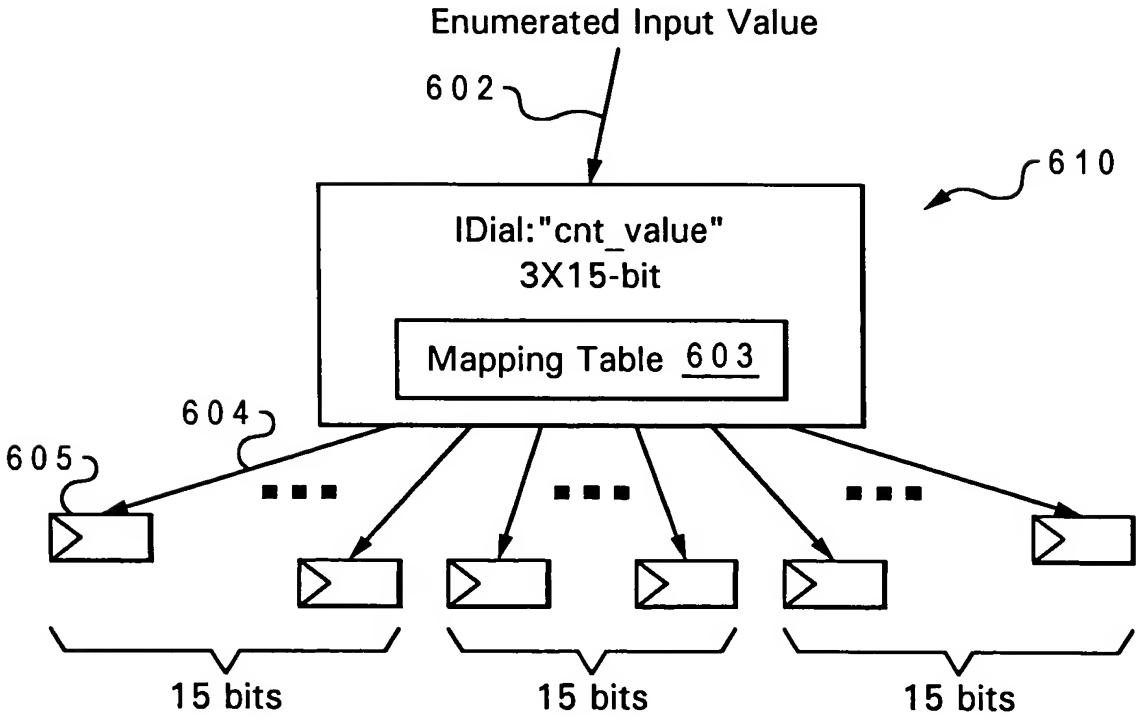

Enumerated Input Value
602
610
IDial:"cnt_value"
3X15-bit
Mapping Table 603
604
605
15 bits
15 bits
15 bits

Fig. 6B

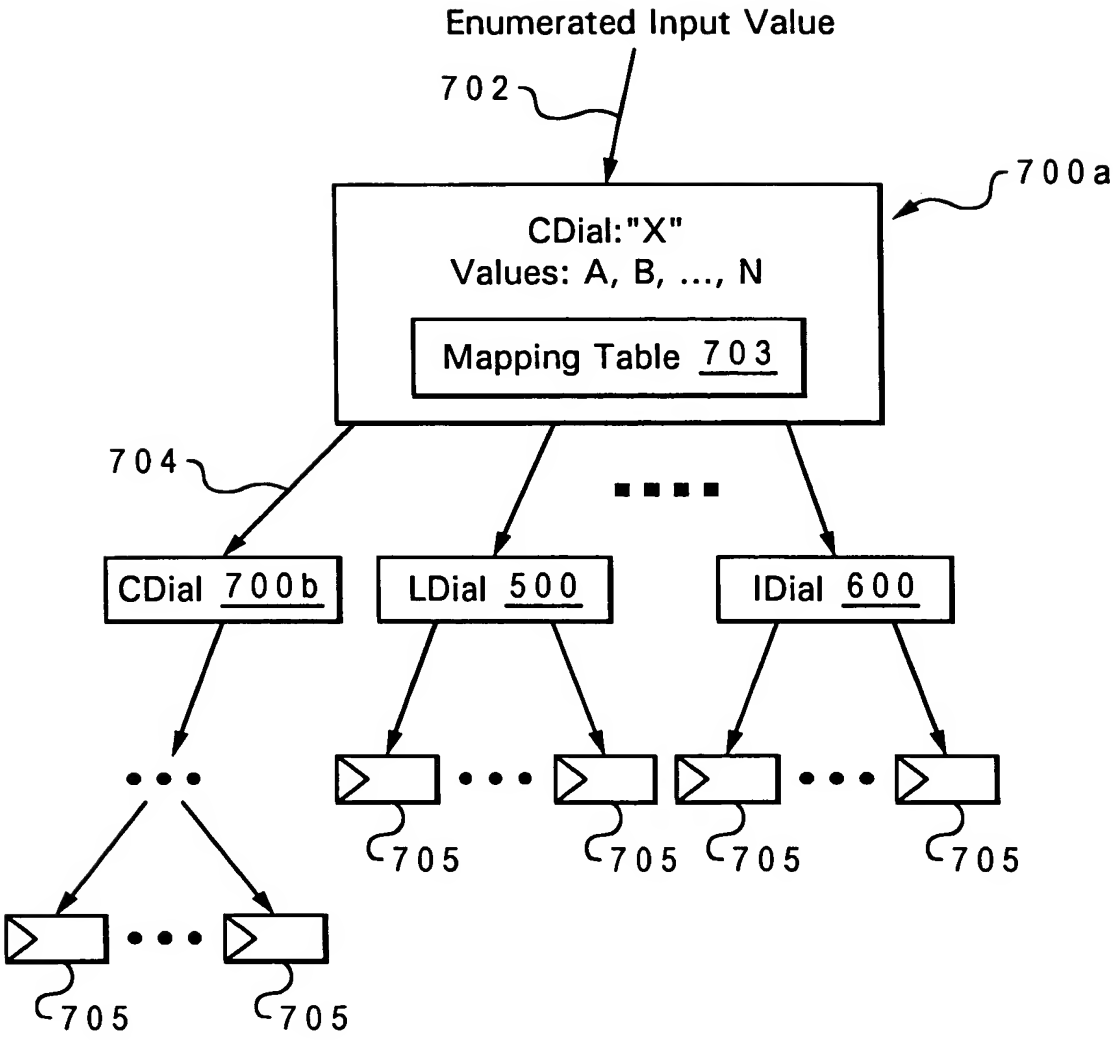

Enumerated Input Value
702
700a
CDial:"X"
Values: A, B, ..., N
Mapping Table 703
704
CDial 700b
LDial 500
IDial 600
705
705
705
705
705
705

Fig. 7A

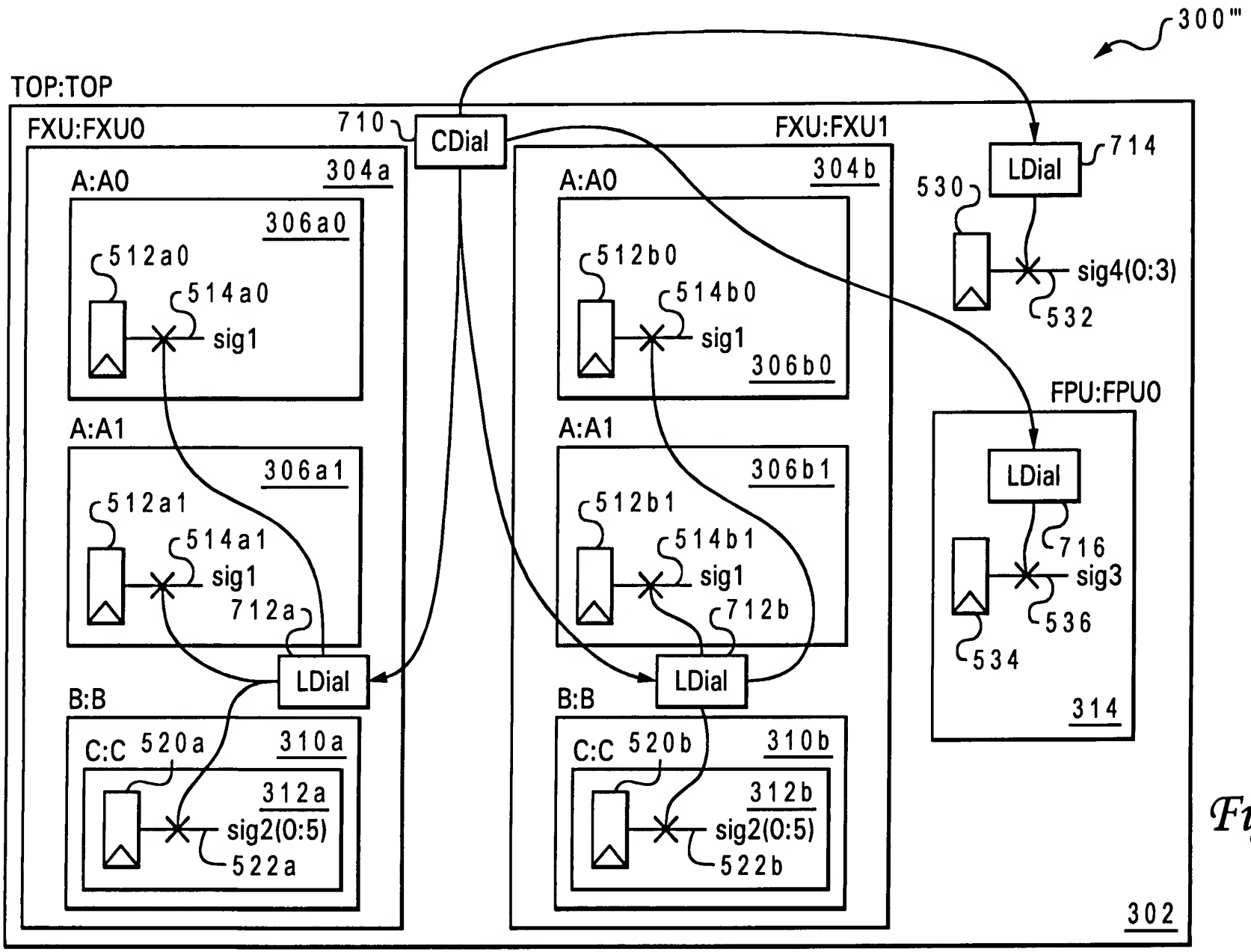

300'''
TOP:TOP
FXU:FXU0
710
CDial
FXU:FXU1
714
LDial
530
A:A0
304a
306a0
512a0
514a0
sig1
A:A0
304b
512b0
514b0
sig1
306b0
sig4(0:3)
532
FPU:FPU0
A:A1
306a1
512a1
514a1
sig1
712a
A:A1
306b1
512b1
514b1
sig1
712b
LDial
716
sig3
536
534
314
LDial
LDial
B:B
C:C
520a
310a
312a
sig2(0:5)
522a
B:B
C:C
520b
310b
312b
sig2(0:5)
522b
302

Fig. 7B

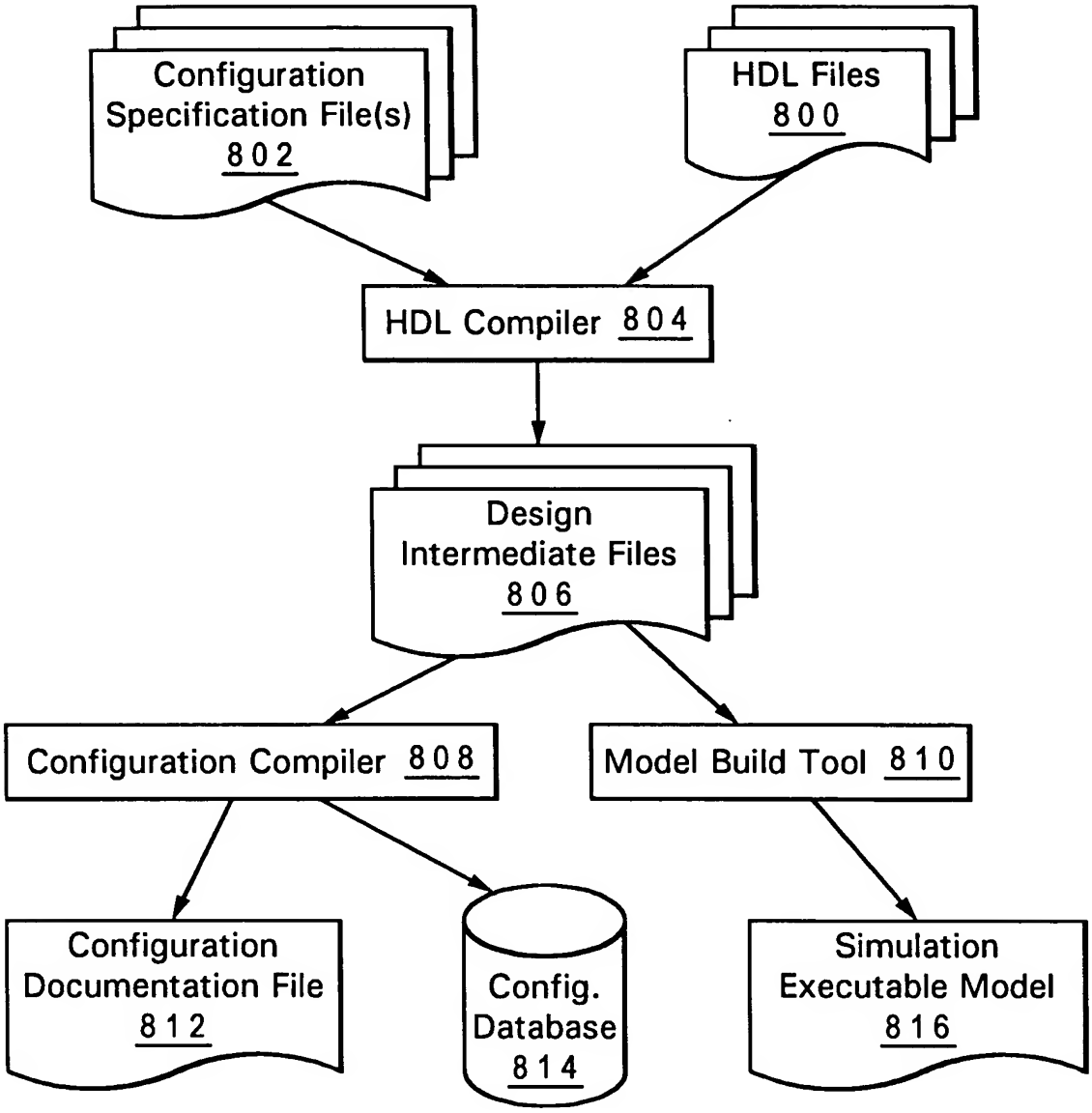

Configuration Specification File(s) 802
HDL Files 800
HDL Compiler 804
Design Intermediate Files 806
Configuration Compiler 808
Model Build Tool 810
Configuration Documentation File 812
Config. Database 814
Simulation Executable Model 816

Fig. 8

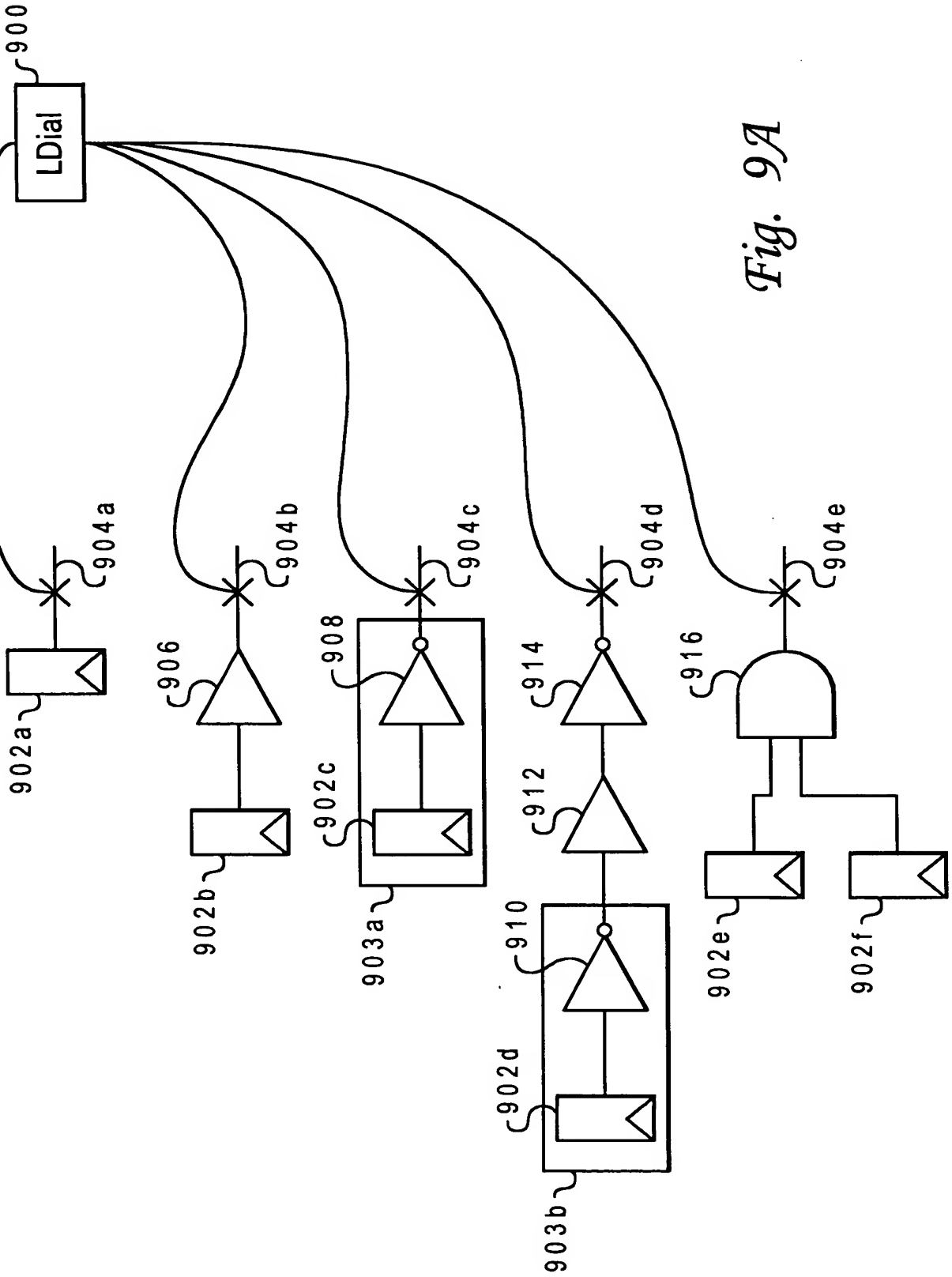

900
LDial
904a
904b
904c
904d
904e
902a
906
902b
908
902c
903a
914
912
910
902d
903b
916
902e
902f

Fig. 9A

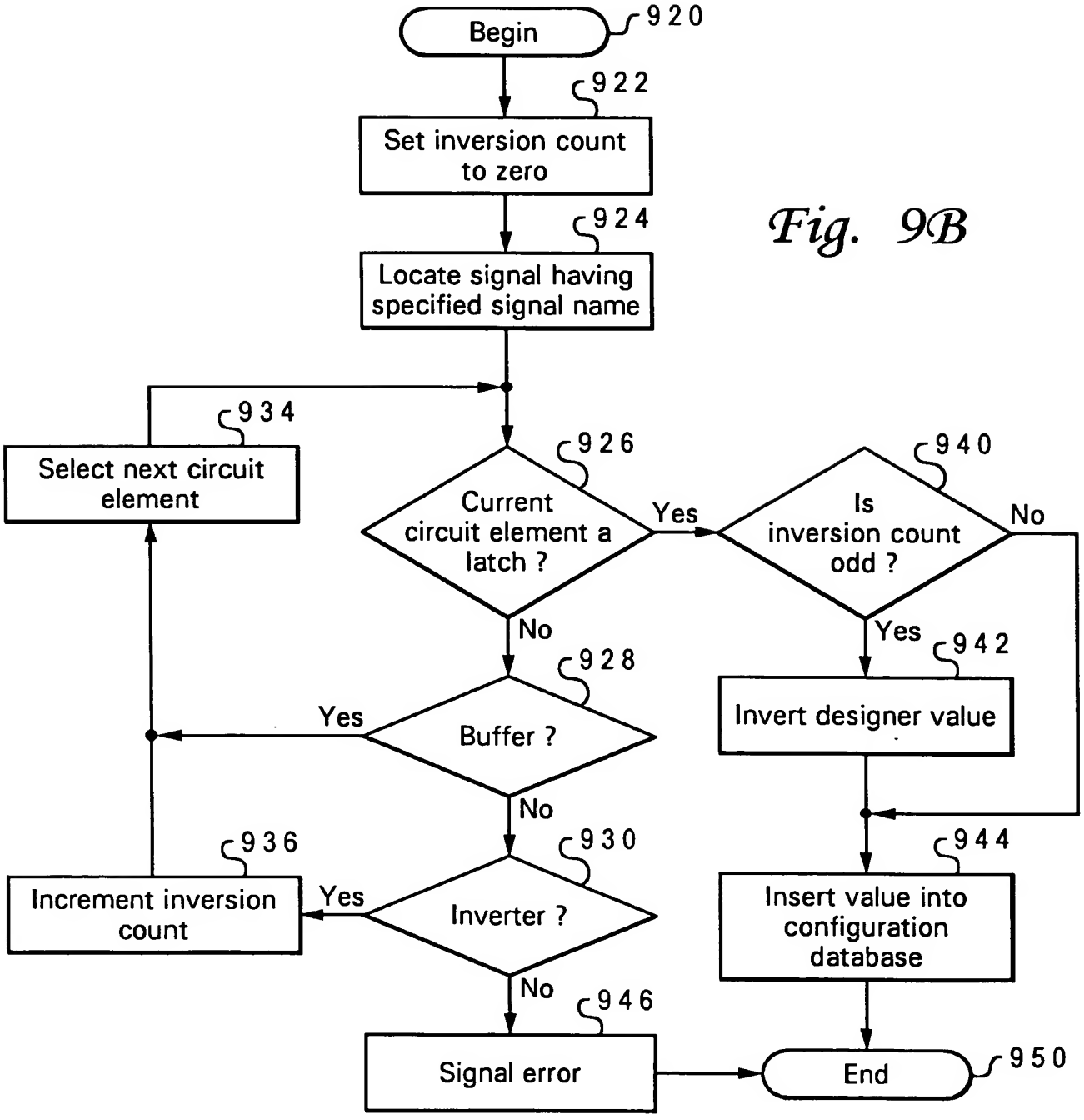

Begin
920
922
Set inversion count to zero
924
Locate signal having specified signal name
926
Current circuit element a latch ?
Yes
940
Is inversion count odd ?
No
No
Yes
942
Invert designer value
928
Buffer ?
Yes
No
930
Inverter ?
Yes
934
Select next circuit element
936
Increment inversion count
944
Insert value into configuration database
No
946
Signal error
End
950

Fig. 9B

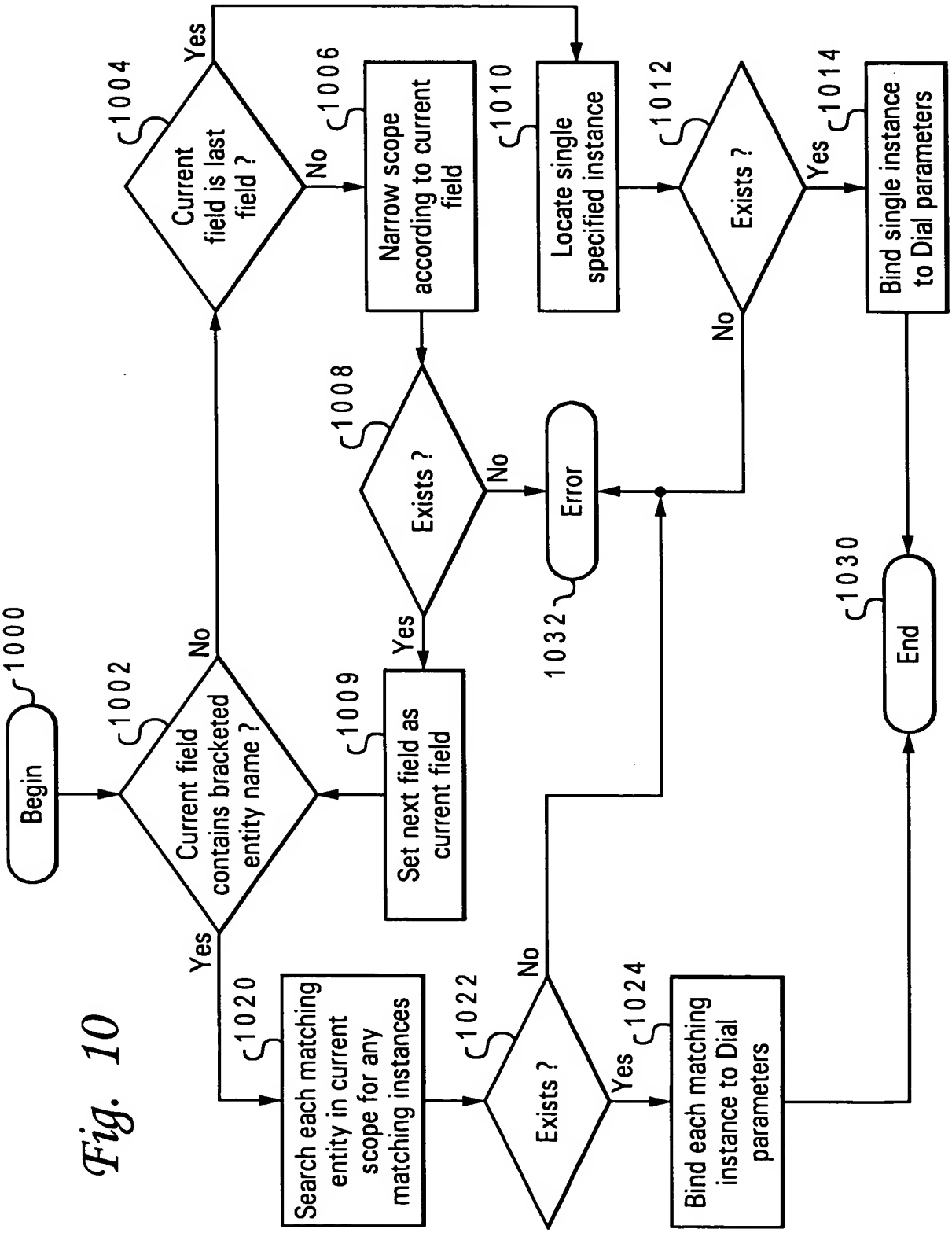

1000
Begin
1002
Current field contains bracketed entity name ?
Yes
No
1004
Current field is last field ?
Yes
No
1006
Narrow scope according to current field
1008
Exists ?
Yes
No
1009
Set next field as current field
1010
Locate single specified instance
1012
Exists ?
Yes
No
1014
Bind single instance to Dial parameters
1020
Search each matching entity in current scope for any matching instances
1022
Exists ?
Yes
No
1024
Bind each matching instance to Dial parameters
1030
End
1032
Error

Fig. 10

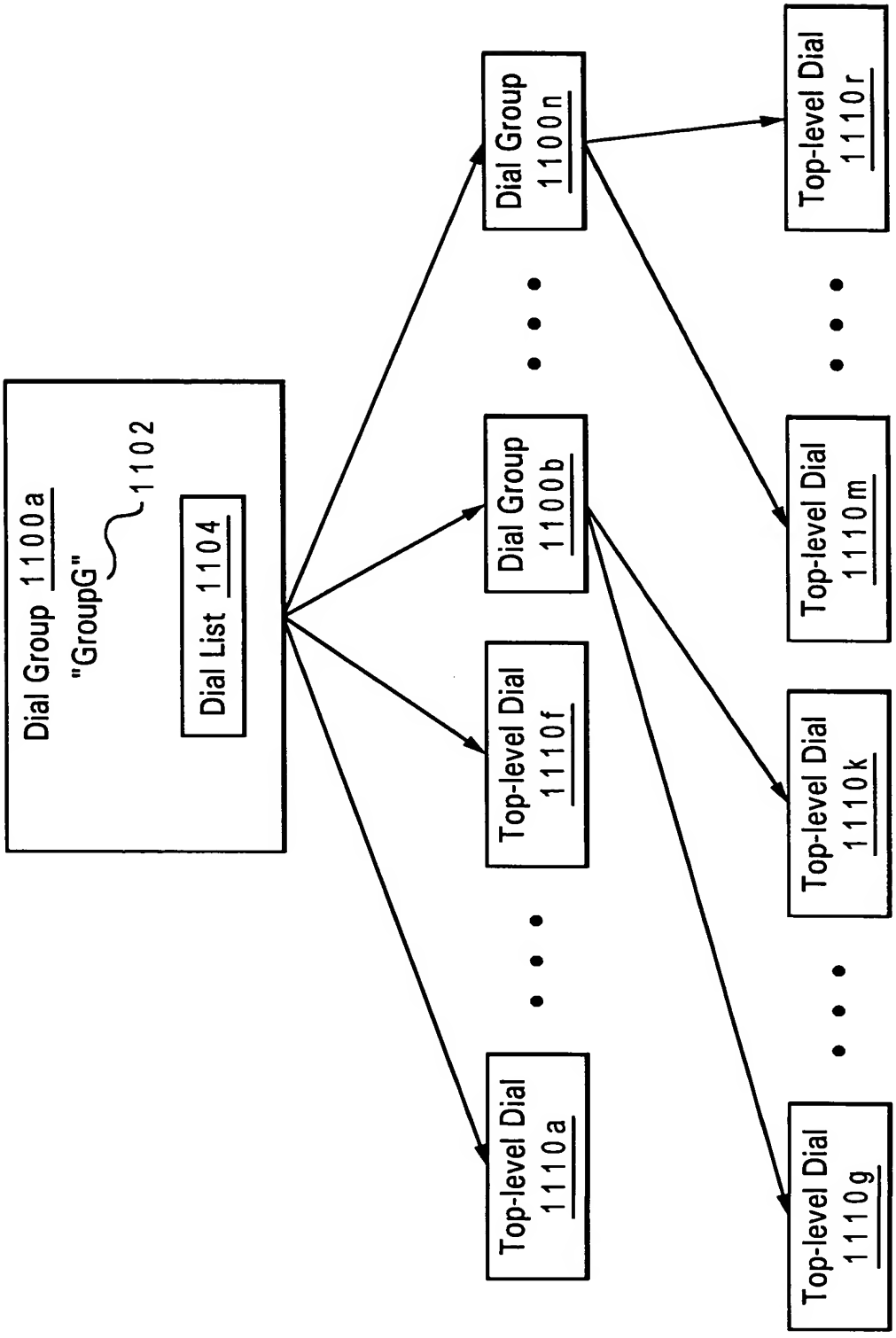

Dial Group 1100a
"GroupG"
1102
Dial List 1104
Top-level Dial 1110a
Top-level Dial 1110f
Dial Group 1100b
Dial Group 1100n
Top-level Dial 1110g
Top-level Dial 1110k
Top-level Dial 1110m
Top-level Dial 1110r

Fig. 11A

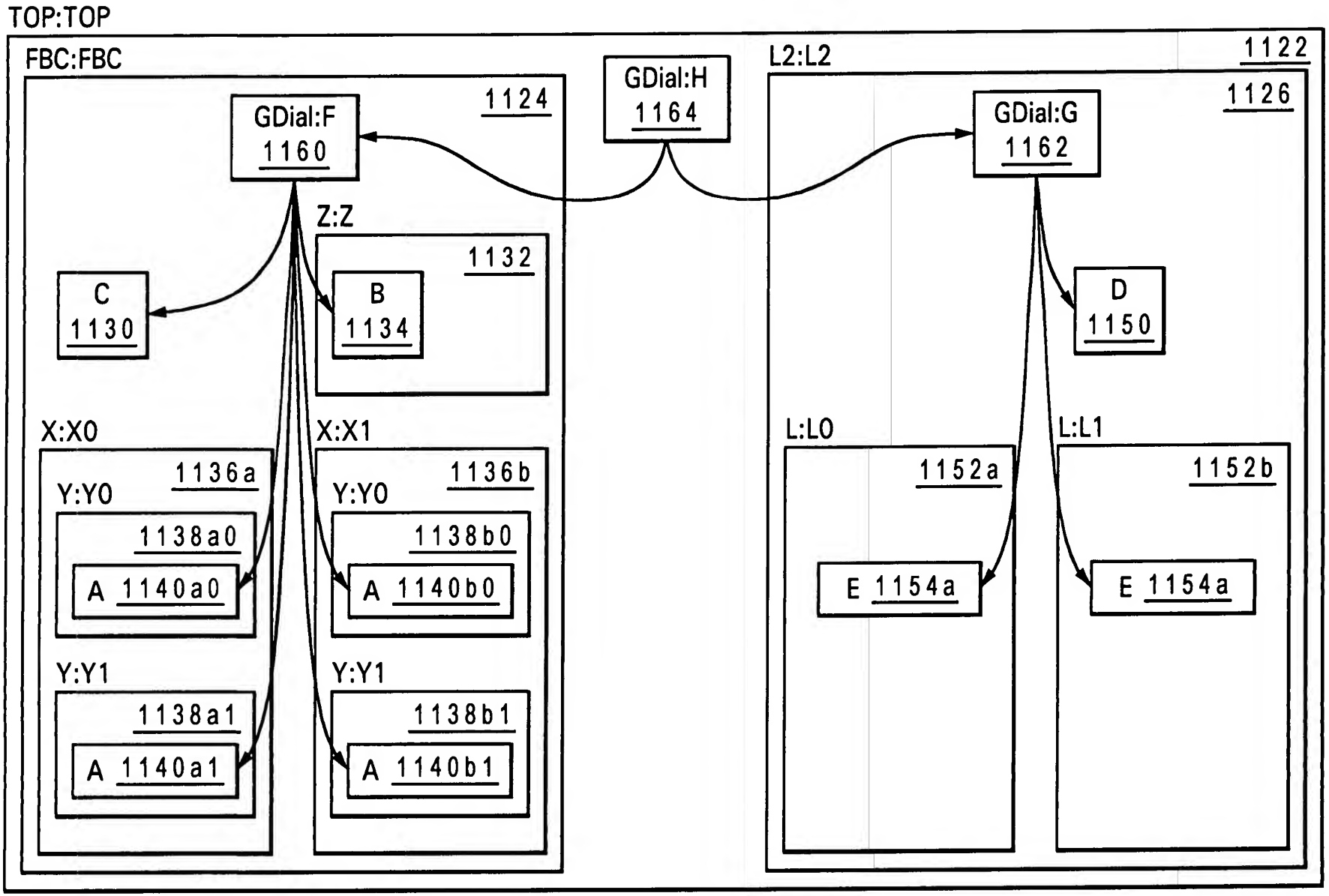
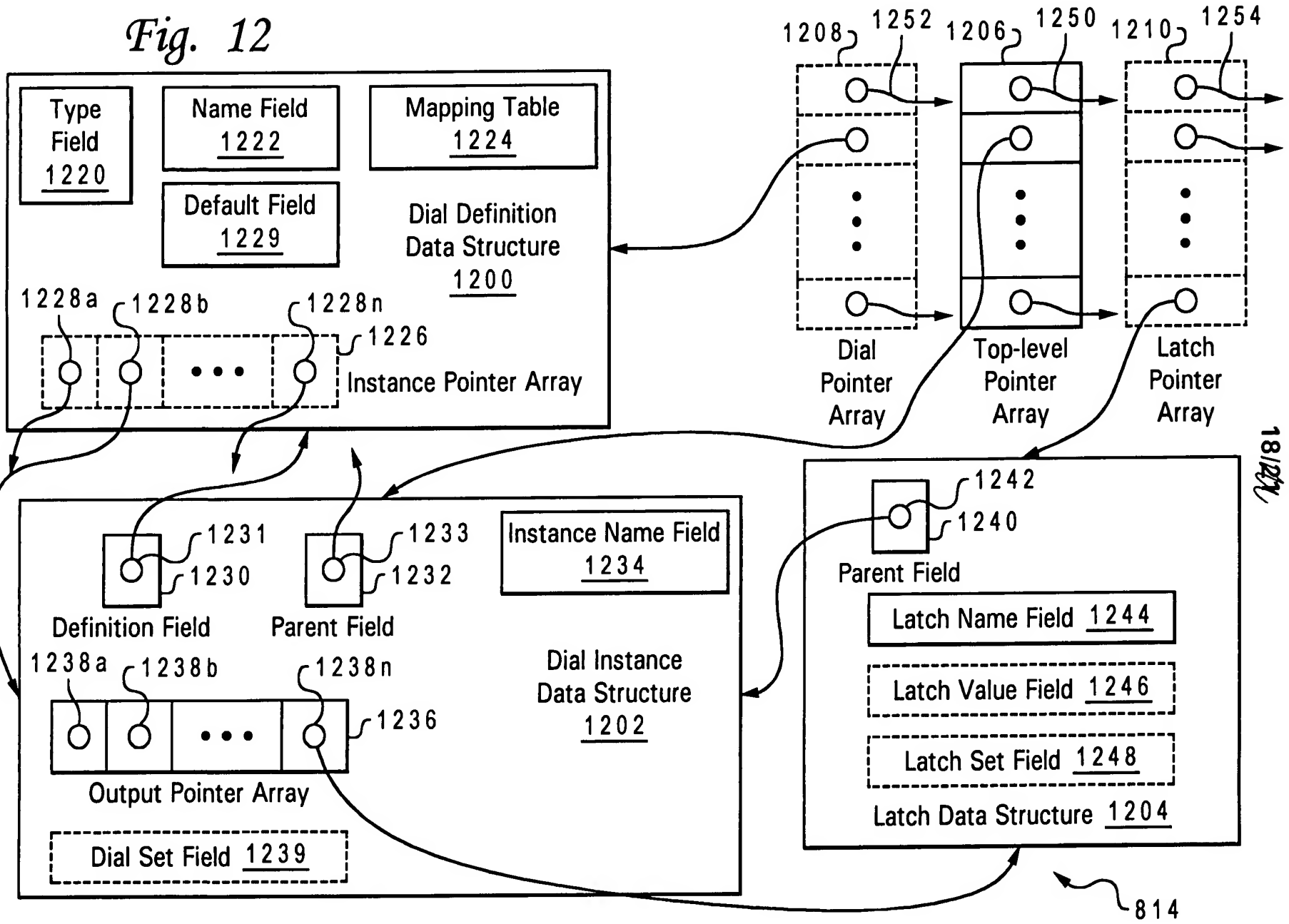

TOP:TOP
FBC:FBC
1124
GDial:F
1160
GDial:H
1164
L2:L2
1122
1126
GDial:G
1162
Z:Z
1132
C
1130
B
1134
D
1150
X:X0
X:X1
L:L0
L:L1
1136a
1136b
Y:Y0
Y:Y0
1138a0
1138b0
A 1140a0
A 1140b0
1152a
1152b
E 1154a
E 1154a
Y:Y1
Y:Y1
1138a1
1138b1
A 1140a1
A 1140b1
1120

Fig. 11B

Fig. 12


Type Field 1220
Name Field 1222
Mapping Table 1224
Default Field 1229
Dial Definition Data Structure 1200
1228a
1228b
1228n
1226
Instance Pointer Array
1208
1252
1206
1250
1210
1254
Dial Pointer Array
Top-level Pointer Array
Latch Pointer Array
1231
1230
1233
1232
Instance Name Field 1234
Definition Field
Parent Field
1238a
1238b
1238n
1236
Output Pointer Array
Dial Instance Data Structure 1202
Dial Set Field 1239
1242
1240
Parent Field
Latch Name Field 1244
Latch Value Field 1246
Latch Set Field 1248
Latch Data Structure 1204
814
18/24

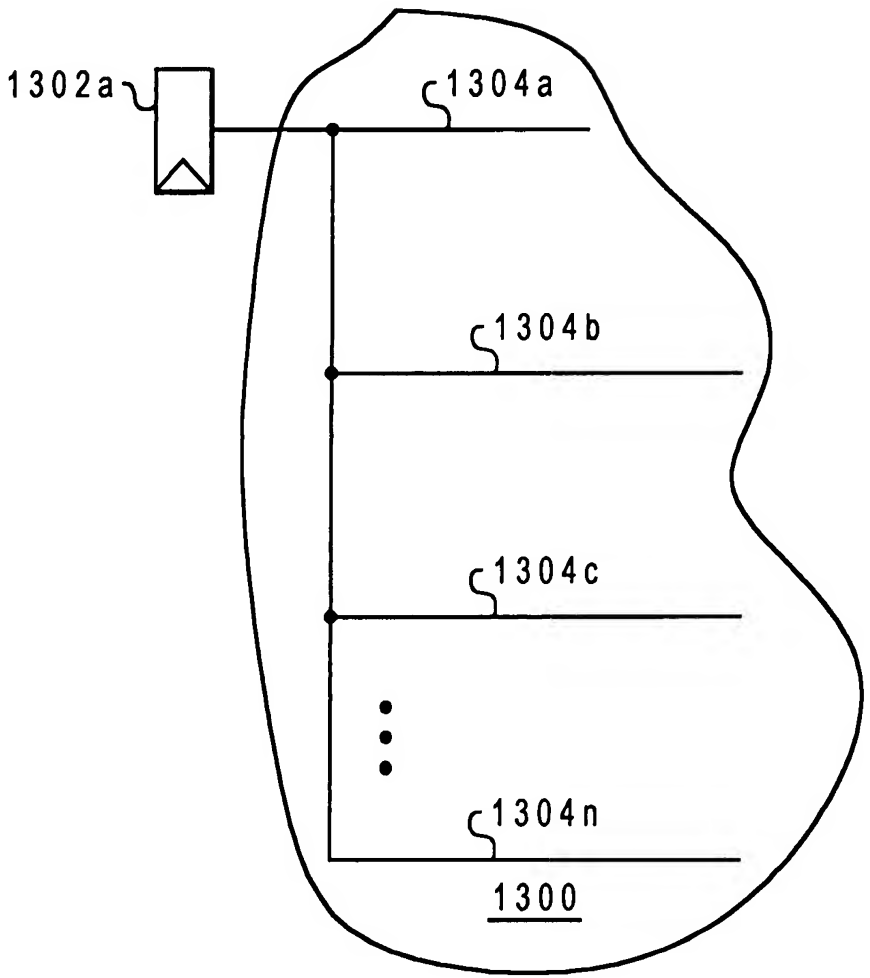


Fig. 13A

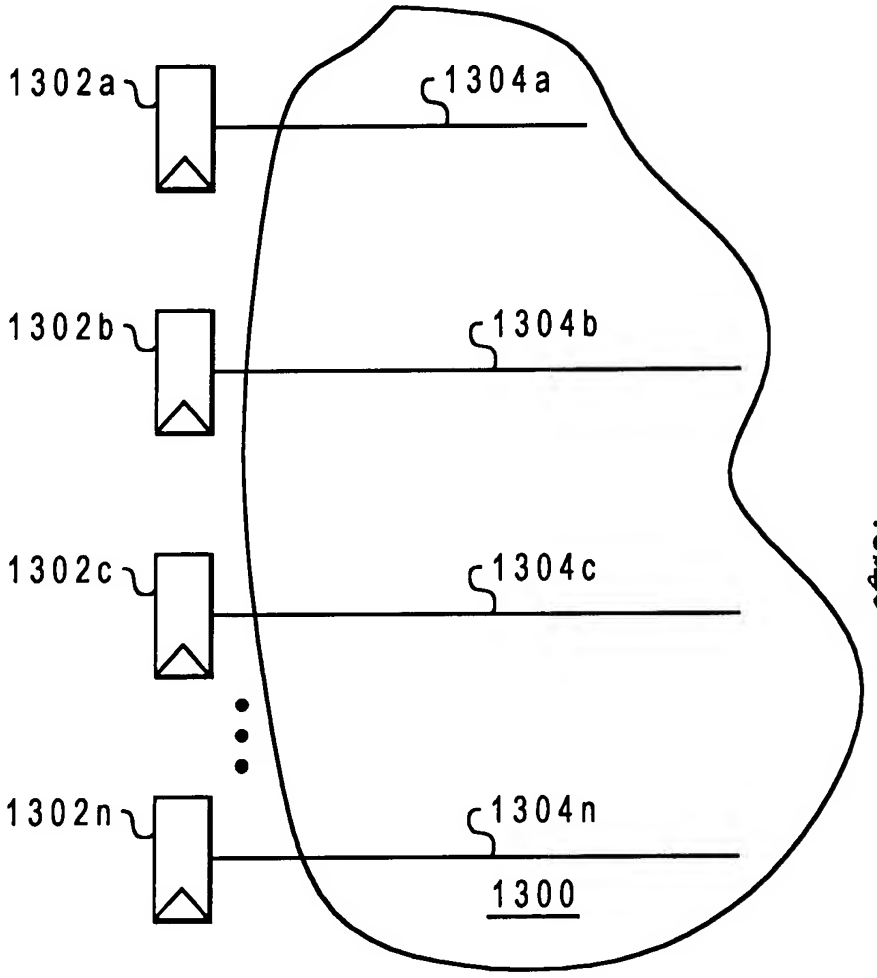


Fig. 13B

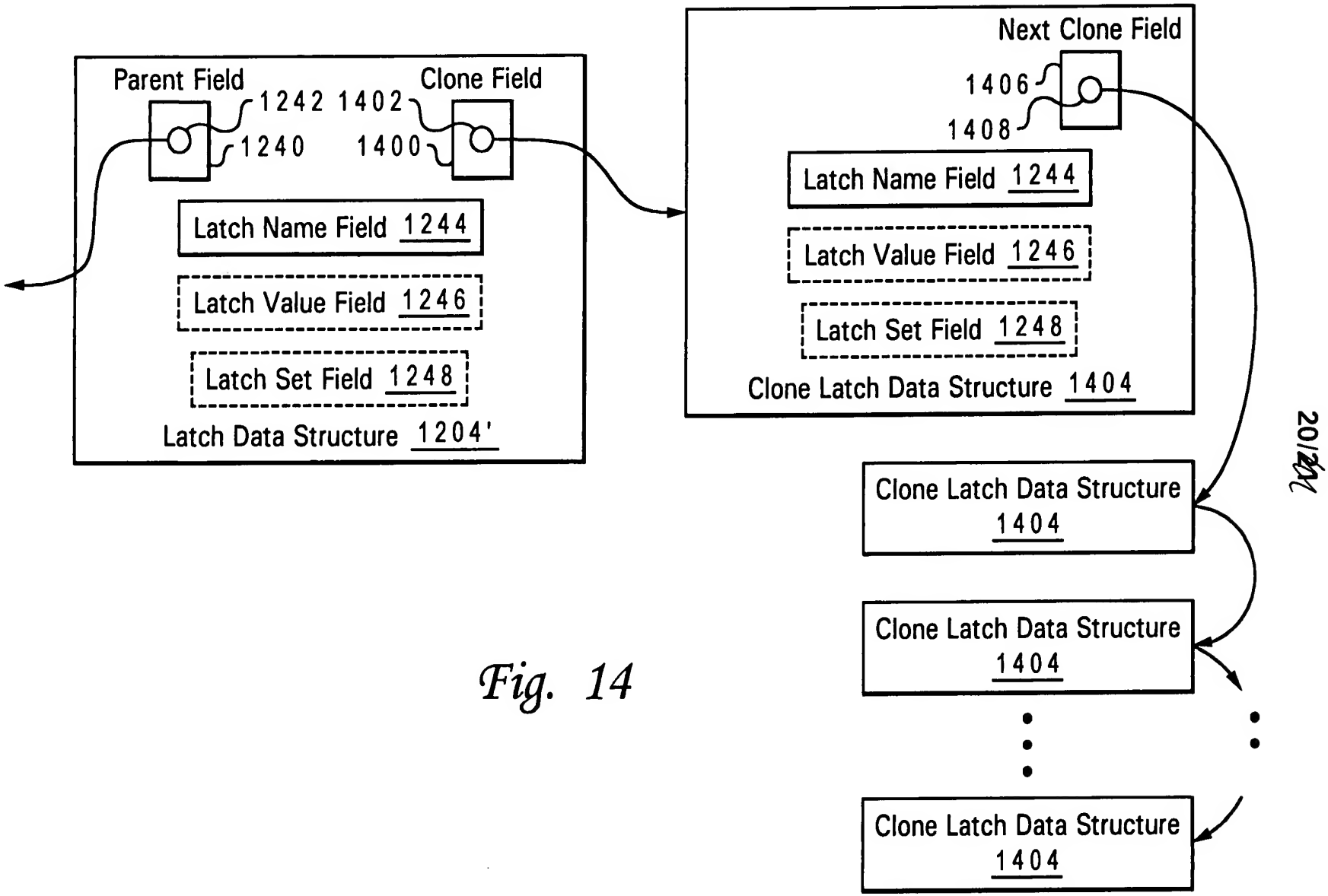

Parent Field
1242
1240
Clone Field
1402
1400
Latch Name Field 1244
Latch Value Field 1246
Latch Set Field 1248
Latch Data Structure 1204'
Next Clone Field
1406
1408
Latch Name Field 1244
Latch Value Field 1246
Latch Set Field 1248
Clone Latch Data Structure 1404
Clone Latch Data Structure 1404
Clone Latch Data Structure 1404
Clone Latch Data Structure 1404
202

Fig. 14

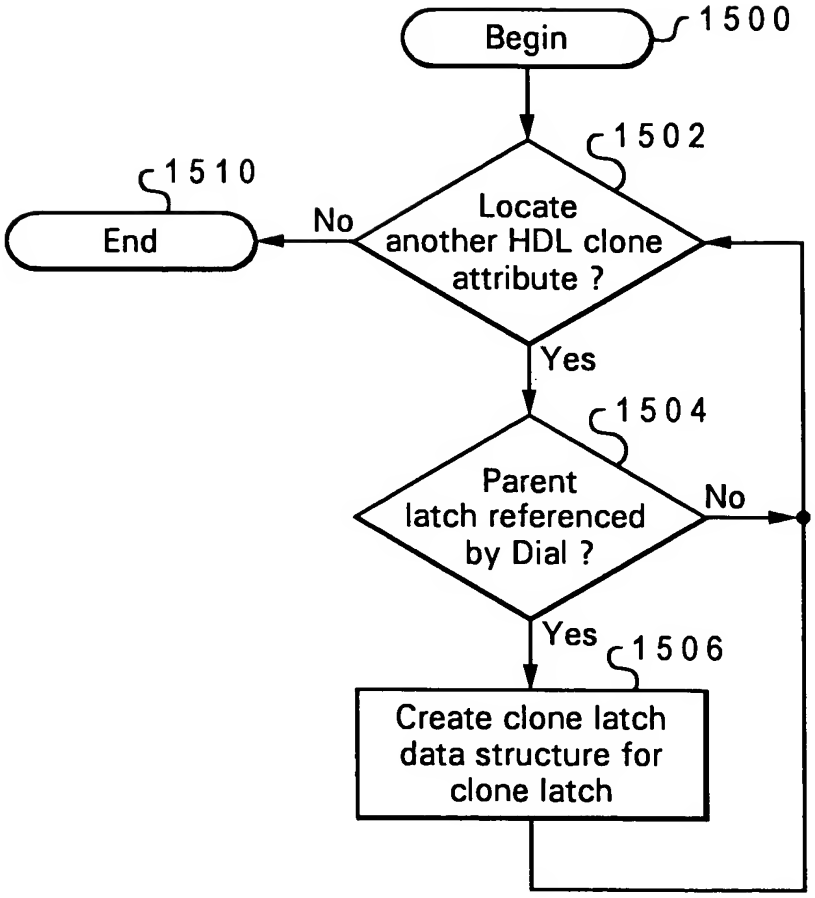

Begin
1500
1502
Locate another HDL clone attribute ?
No
1510
End
Yes
1504
Parent latch referenced by Dial ?
No
Yes
1506
Create clone latch data structure for clone latch

Fig. 15

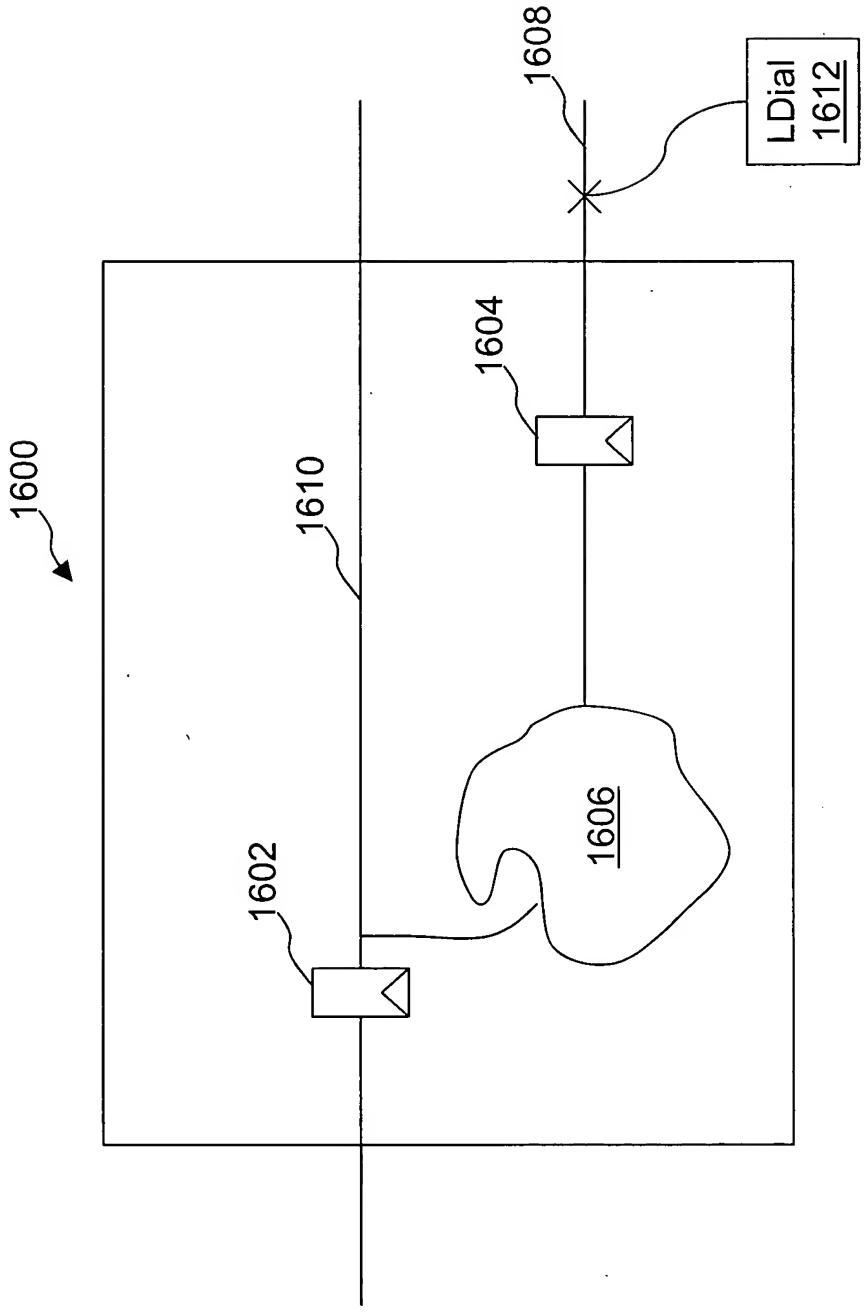


Figure 16A

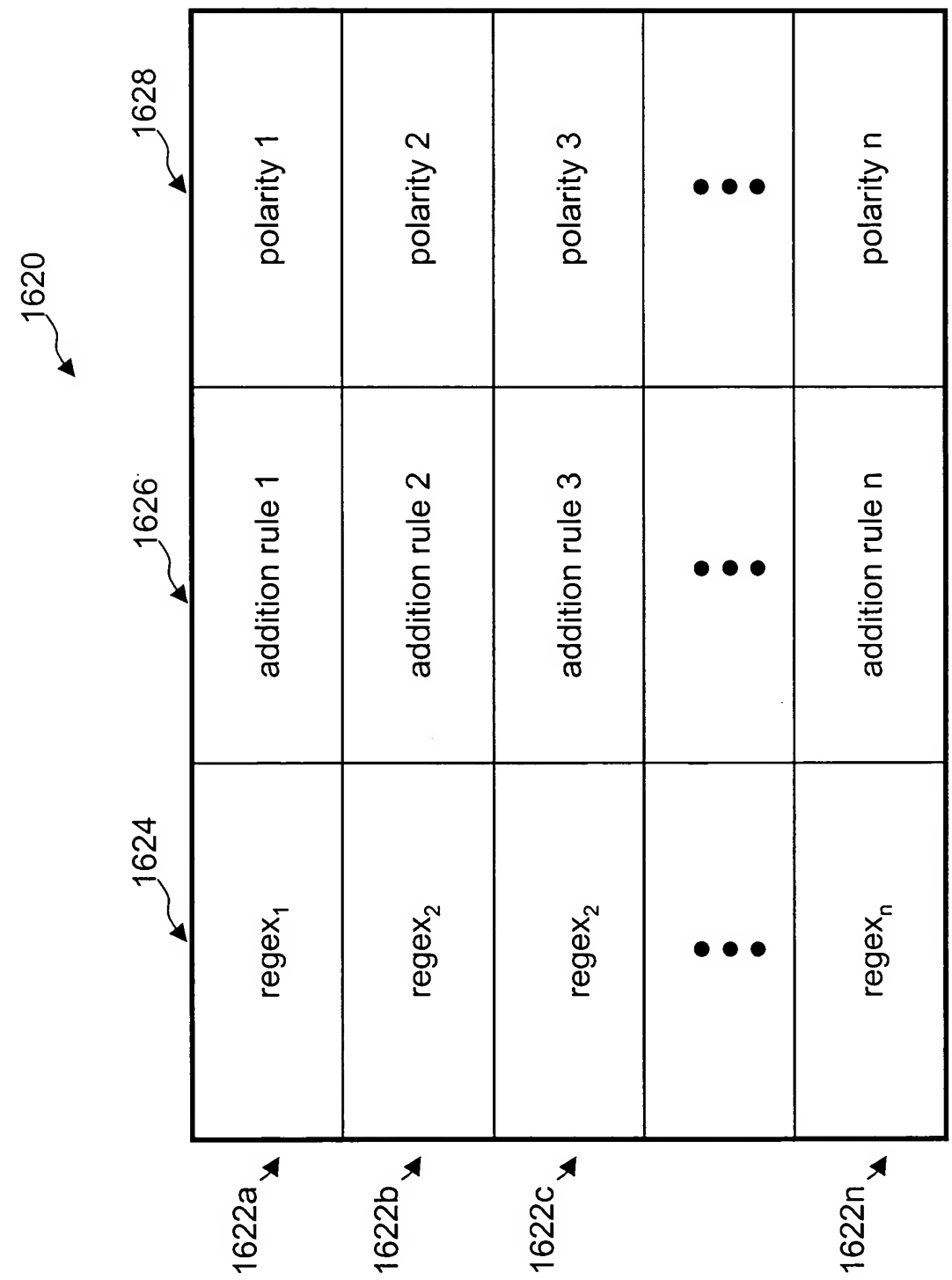

1620
1624
1626
1628
1622a
1622b
1622c
1622n
regex1
regex2
regex2
regexn
addition rule 1
addition rule 2
addition rule 3
addition rule n
polarity 1
polarity 2
polarity 3
polarity n

Figure 16B

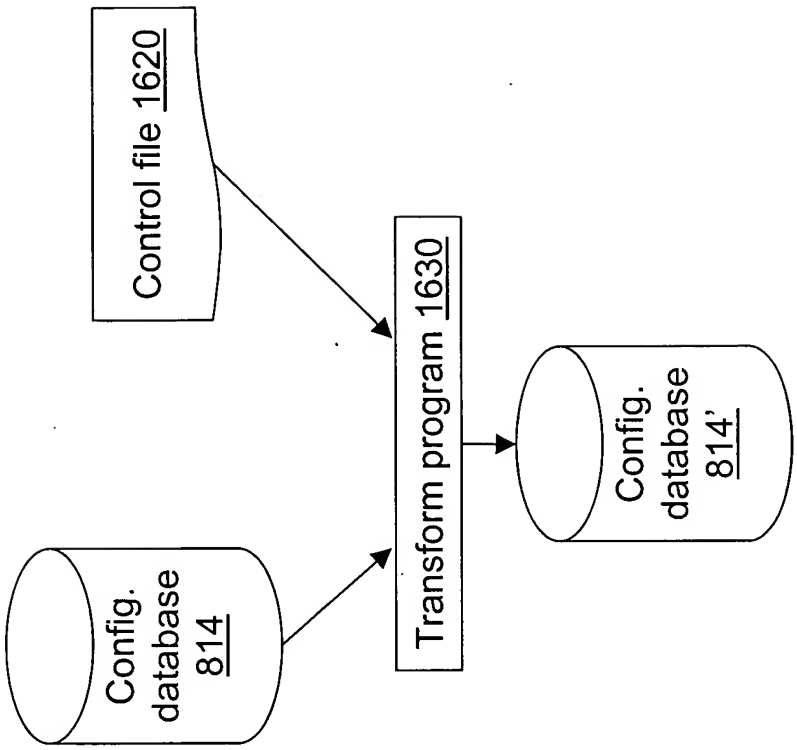

Control file 1620
Transform program 1630
Config. database 814
Config. database 814'

Figure 16C

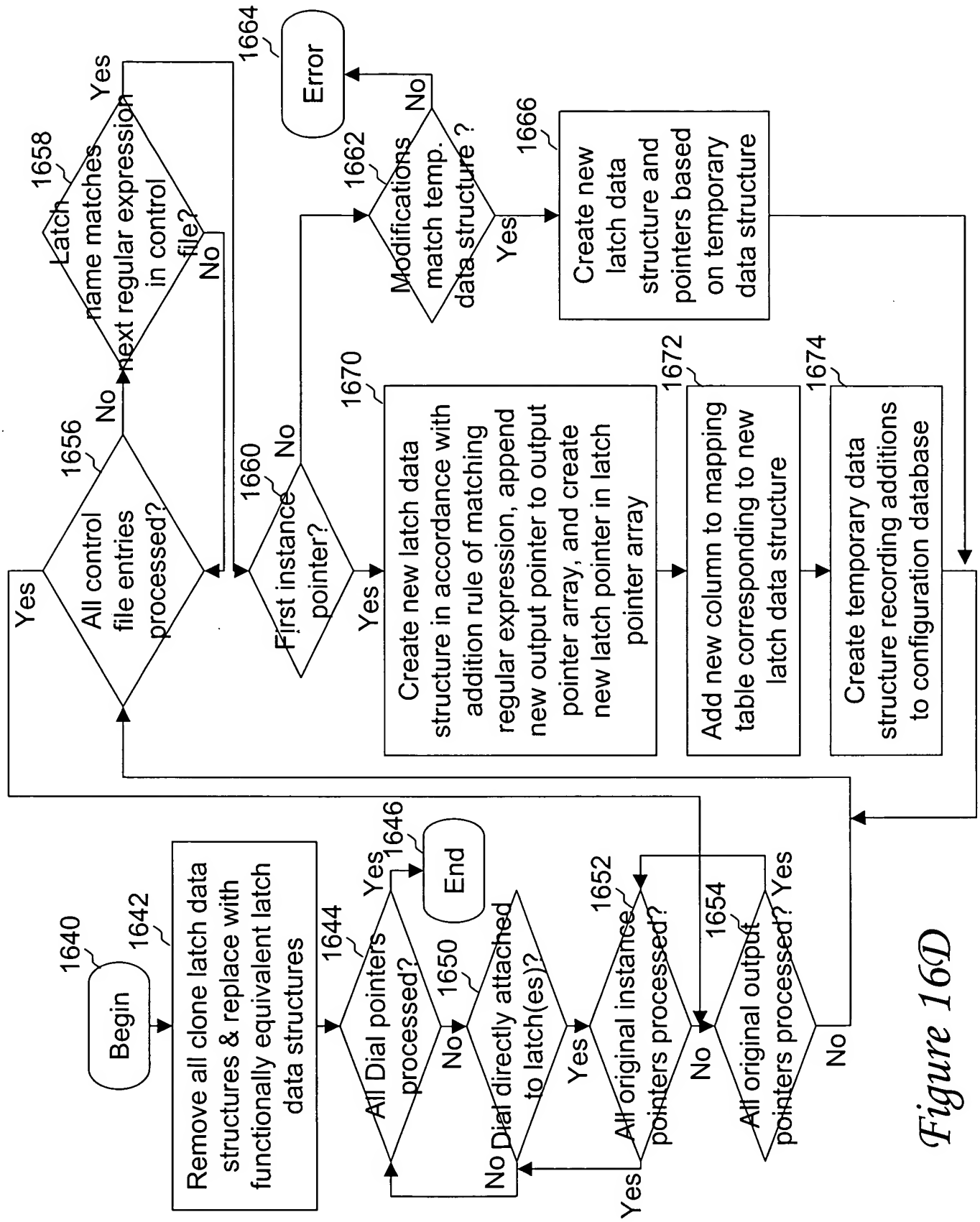

1640
Begin
1642
Remove all clone latch data structures & replace with functionally equivalent latch data structures
1644
All Dial pointers processed?
Yes
1646
End
No
1650
Dial directly attached to latch(es)?
No
Yes
1652
All original instance pointers processed?
Yes
No
1654
All original output pointers processed?
Yes
No
1656
All control file entries processed?
Yes
No
1658
Latch name matches next regular expression in control file?
Yes
No
1660
First instance pointer?
No
Yes
1662
Modifications match temp. data structure ?
No
Yes
1664
Error
1666
Create new latch data structure and pointers based on temporary data structure
1670
Create new latch data structure in accordance with addition rule of matching regular expression, append new output pointer to output pointer array, and create new latch pointer in latch pointer array
1672
Add new column to mapping table corresponding to new latch data structure
1674
Create temporary data structure recording additions to configuration database

Figure 16D